

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first transistor having a gate insulating film of a first thickness, at least one of source/drain of said first transistor being formed of a first lightly doped region and a first heavily doped region; and

a second transistor having a gate insulating film of a second thickness smaller than said first thickness, at least one of source/drain of said second transistor including a second lightly doped region and a second heavily doped region higher in concentration than said first heavily doped region.

2. The semiconductor device according to claim 1, wherein

at least one of the source/drain of said second transistor has a medium-doped region having a concentration higher than said second lightly doped region and lower than said second heavily doped region.

3. The semiconductor device according to claim 1, wherein

said semiconductor device includes a memory cell portion for storing data and a peripheral circuit portion

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5 for external input/output,  
said memory cell portion includes said first transistor,  
and  
said peripheral circuit portion includes said second  
transistor.

4. The semiconductor device according to claim 2,  
wherein  
a diffusion depth of said second heavily doped region  
is smaller than a diffusion depth of said medium-doped  
5 region.

5. The semiconductor device according to claim 1,  
wherein  
a field insulating film is formed in contact with said  
first heavily doped region,

5 said first and second transistors are covered with an  
interlayer insulating film having a contact hole reaching  
said first heavily doped region and said field insulating  
film, and

10 a concavity is formed at said field insulating film  
located immediately under said contact hole, and

a storage node is formed in said concavity and on said  
first heavily doped region.

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6. A semiconductor device comprising:

a semiconductor substrate having a main surface;

a first impurity region for threshold voltage control having a peak concentration at a position of a first depth from said main surface;

a second impurity region for threshold voltage control spaced from said first impurity region, and having a peak concentration at a position of a second depth larger than said first depth;

a first transistor formed on said first impurity region, and having a gate insulating film of a first thickness; and

a second transistor formed on said second impurity region, and having a gate insulating film of a second thickness smaller than said first thickness;

7. The semiconductor device according to claim 6, wherein

a third impurity region lower in concentration than said first impurity region is formed under said first impurity region,

said first transistor has a pair of first source/drain, at least one of said first source/drain reaches said third impurity region,

said second transistor has a pair of second source/drain, and

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said second source/drain have diffusion depths smaller than said second depth.

8. A semiconductor device comprising:

5 a first transistor having a gate insulating film of a first thickness, and having first and second impurity regions having relatively large first diffusion depth and relatively small second diffusion depth and forming source/drain, respectively, and;

10 a second transistor having a gate insulating film of a second thickness smaller than said first thickness, and having third and fourth diffusion regions having diffusion depths smaller than said first diffusion depth and not smaller than said second diffusion depth, and forming source/drain, respectively.

9. The semiconductor device according to claim 8, wherein

5 a concentration of said first impurity region having said first diffusion depth is higher than a concentration of said second impurity region, and a field insulating film is formed in contact with said first impurity region.

10. A semiconductor device comprising:

a first transistor formed on a main surface of a

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semiconductor substrate, and having first source/drain;

5 a second transistor formed on said main surface with a space from said first transistor, and having second source/drain;

an interlayer insulating film covering said first and second transistors, and having a contact hole reaching one of said first source/drain;

10 a plug electrode formed in said contact hole;

first metal silicide formed on surfaces of said second source/drain; and

a bit line formed on said plug electrode with a second metal silicide therebetween.

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